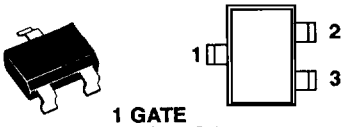
SST201 SERIES
N-Channel JFETs

The SST201 Series is the SOT-23 equivalent of our popular J201 Series. It features low leakage, very low noise, and low cutoff voltage for use with low level power supplies. The SST201 is excellent for battery operated equipment and low current amplifiers. The SST201 Series SOT-23 package affords low cost and compatibility with automated assembly techniques. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
SST201	-1.5	-40	0.5	1
SST202	-4	-40	1	4.5

For further design information please consult the typical performance curves NPA.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J201 Series
- TO-18, See 2N4338 Series
- Chips, See NPA Series Die

PRODUCT MARKING	
SST201	P01
SST202	P02

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-40	V
Gate-Source Voltage	V_{GS}	-40	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

4

SPECIFICATIONS[a]			LIMITS					
				SST201		SST202		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA		-0.3	-1.5	-0.8	-4	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.2	1	0.9	4.5	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -20 V, V_{DS} = 0 V	-2		-100		-100	pA
		T_A = 125°C	-1					nA
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 0.1 mA	-2					pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 15 V, V_{GS} = -10 V	2					
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7					V
DYNAMIC								
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, V_{GS} = 0 V f = 1 kHz		0.5		1		mS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V f = 1 MHz	4.5					pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3					
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V f = 1 kHz	6					$nV/\sqrt{Hz}$

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle $\leq$ 3%.